Smoothing Gate Capacitance Models for CMOS Radio Frequency and Microwave Integrated Circuits CAD

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Abstract — **Convergence problems for both voltage- and charge-controlled models of MOSFET gate capacitances are often a limiting factor of CAD tools. In paper, an idea of exponential smoothing of model discontinuities is proposed. The method is demonstrated by smoothing the discontinuity of Meyer's model at zero drain-source voltage. The updated model is tested on flip-flop circuit by an advanced algorithm.**

I. Introduction

The gate capacitance models have been defined precisely concerning gate-source voltage. However, models need a refinement for a case of large drain-source variation — it will be demonstrated on a CMOS flip-flop circuit analysis by author's C.I.A. (Circuit Interactive Analyzer) program.

II. Definition of a Necessity to Ensure Convergence

The SPICE3 program has implemented Meyer's voltage controlled model, the programs of PSPICE family contain the same model and Ward's charge controlled model in several levels, especially for BSIM class. In most cases, the models have not problems relative to gate-source voltage changes. However, if drain-source voltage exchanges sign during transient analysis, convergence problems can occur. Such problems are described in [2, p. 197] for the Meyer's model and in [2, p. 198] for the Ward's models. For that reason, a requirement for an updated model can be defined

$$\lim_{V_{DS}\to 0+} C_{GS} = \lim_{V_{DS}\to 0-} C_{GS} \wedge \lim_{V_{DS}\to 0+} C_{GD} = \lim_{V_{DS}\to 0-} C_{GD} \quad (1)$$

and $$\lim_{V_{DS}\to 0+} \dot{Q}_S = \lim_{V_{DS}\to 0-} \dot{Q}_S \wedge \lim_{V_{DS}\to 0+} \dot{Q}_D = \lim_{V_{DS}\to 0-} \dot{Q}_D \quad (2)$$

for the Meyer's and Ward's model, respectively.

III. Definition of Discontinuities of Classical Model

The discontinuity problem can well be defined on classical Meyer's model that is discussed in a simple form in [1] and in a quite complete form in [2]. However, the actual implementation in the SPICE program slightly differs from [2]. Hence, let define the updated model in a complete way with the discontinuities to be under consideration. The definition for normal mode ($V_{DS} \geq 0$) is divided to 5 regions:

- for $V_{GS} - V_{on} \leq -\phi_S$ (*accumulation* region):

$$\begin{aligned} C_{GB} &= C_{ox}, \\ C_{GS} &= 0, \\ C_{GD} &= 0, \end{aligned} \quad (3)$$

- for $-\phi_S < V_{GS} - V_{on} \leq -\frac{\phi_S}{2}$ (*transition* region):

$$\begin{aligned} C_{GB} &= -C_{ox}\frac{V_{GS}-V_{on}}{\phi_S}, \\ C_{GS} &= 0, \\ C_{GD} &= 0, \end{aligned} \quad (4)$$

- for $-\frac{\phi_S}{2} < V_{GS} - V_{on} \leq 0$ (*depletion* region):

$$\begin{aligned} C_{GB} &= -C_{ox}\frac{V_{GS}-V_{on}}{\phi_S}, \\ C_{GS} &= \frac{2}{3}C_{ox}\left(2\frac{V_{GS}-V_{on}}{\phi_S}+1\right), \\ C_{GD} &= 0, \end{aligned} \quad (5)$$

- for $0 < V_{GS} - V_{on} \leq V_{DS}$ (*saturation* region):

$$\begin{aligned} C_{GB} &= 0, \\ C_{GS} &= \frac{2}{3}C_{ox}, \\ C_{GD} &= 0, \end{aligned} \quad (6)$$

- for $V_{GS} - V_{on} > V_{DS}$ (*linear* region):

$$\begin{aligned} C_{GB} &= 0, \\ C_{GS} &= \frac{2}{3}C_{ox}\left\{1-\left[\frac{V_{GS}-V_{on}-V_{DS}}{2(V_{GS}-V_{on})-V_{DS}}\right]^2\right\}, \\ C_{GD} &= \frac{2}{3}C_{ox}\left\{1-\left[\frac{V_{GS}-V_{on}}{2(V_{GS}-V_{on})-V_{DS}}\right]^2\right\}. \end{aligned} \quad (7)$$

V_{on} voltage is part of static model and acts as a boundary between regions of the weak and strong inversions, ϕ_S is the surface inversion potential, and C_{ox} is determined by oxide permittivity and thickness, effective channel length and channel width—see Fig. 1:

$$C_{ox} = C'_{ox}L_{eff}W = \frac{\varepsilon_{ox}}{t_{ox}}L_{eff}W. \quad (8)$$

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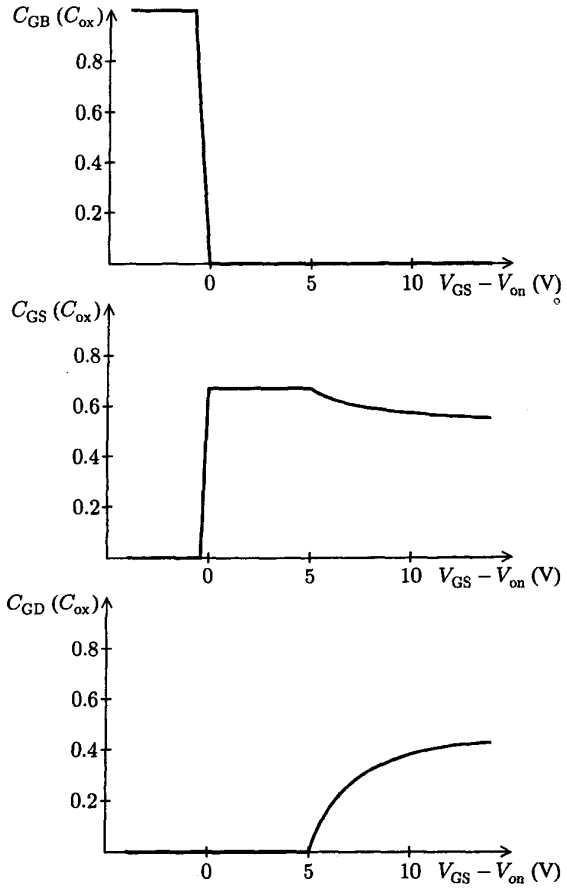

Fig. 1. Updated Meyer's gate capacitance model in C_{ox} units.

We can now easily check that Meyer's modified model defined in (3) to (8) is continuous relative to gate-source voltage. However, if drain-source voltage is changing sign whereas the gate-source voltage remains unchanged then a discontinuity might arise. For a lucid example, suppose the gate-source voltage fulfills the condition for the saturation region (6), i.e. $0 < V_{GS} - V_{on} \leq V_{DS}$ —the discontinuities now arise for both source and drain gate capacitances

$$\lim_{V_{DS}\to 0+} C_{GS} = \lim_{V_{DS}\to 0-} C_{GD} = \frac{2}{3} C_{ox}, \tag{9}$$

$$\lim_{V_{DS}\to 0-} C_{GS} = \lim_{V_{DS}\to 0+} C_{GD} = 0 \tag{10}$$

because the role of C_{GS} and C_{GD} exchanges for $V_{DS} < 0$ in the SPICE models. In other words, it is natural to expect

$$\lim_{V_{DS}\to 0} C_{GS} = \lim_{V_{DS}\to 0} C_{GD} \tag{11}$$

for *symmetrical* device and that condition is *not* kept—(6).

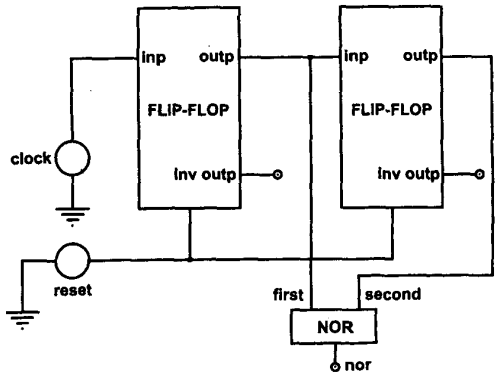

Fig. 2. Simplified schema of probed fraction of a large CMOS integrated circuit.

IV. Solving the Problem by Exponential Smoothing

The problem of discontinuities (9) to (11) can easily be resolved by means of the exponential factor

$$F_G = \exp\left(-\frac{V_{DS}}{n_{smooth} V_T}\right) \quad \text{for} \quad V_{DS} \geq 0 \tag{12}$$

and

$$F_G = \exp\left(\frac{V_{DS}}{n_{smooth} V_T}\right) \quad \text{for} \quad V_{DS} < 0, \tag{13}$$

where n_{smooth} is a new model parameter with unit default value and V_T is thermal voltage. For all the C_{GS} and C_{GD} capacitances in (3) to (7), new ones are defined by

$$C'_{GS} = F_G \frac{C_{GS} + C_{GD}}{2} + (1 - F_G) C_{GS}, \tag{14}$$

$$C'_{GD} = F_G \frac{C_{GS} + C_{GD}}{2} + (1 - F_G) C_{GD} \tag{15}$$

— for symmetrical devices, again. Note that the C_{GB} capacitance has not that discontinuity problem and therefore is left without any changes ($C'_{GB} = C_{GB}$).

In other words, the C'_{GS} and C'_{GD} capacitances have the equal values for $V_{DS} \to 0$ (which must be physical reality for symmetrical devices) now and the original unmodified values for $|V_{DS}| \gg V_T$.

It is also evident that the 50/50 dividing used in (14) and (15) can be generalized for other ratio of gate-source and gate-drain capacitances. Moreover, the analog smoothing method is usable for three partitionings of Ward's model.

V. Test of the Discontinuity Exponential Smoothing

A radio frequency CMOS flip-flop circuit has appeared as a sophisticated test of convergence. Only a part in Fig. 2

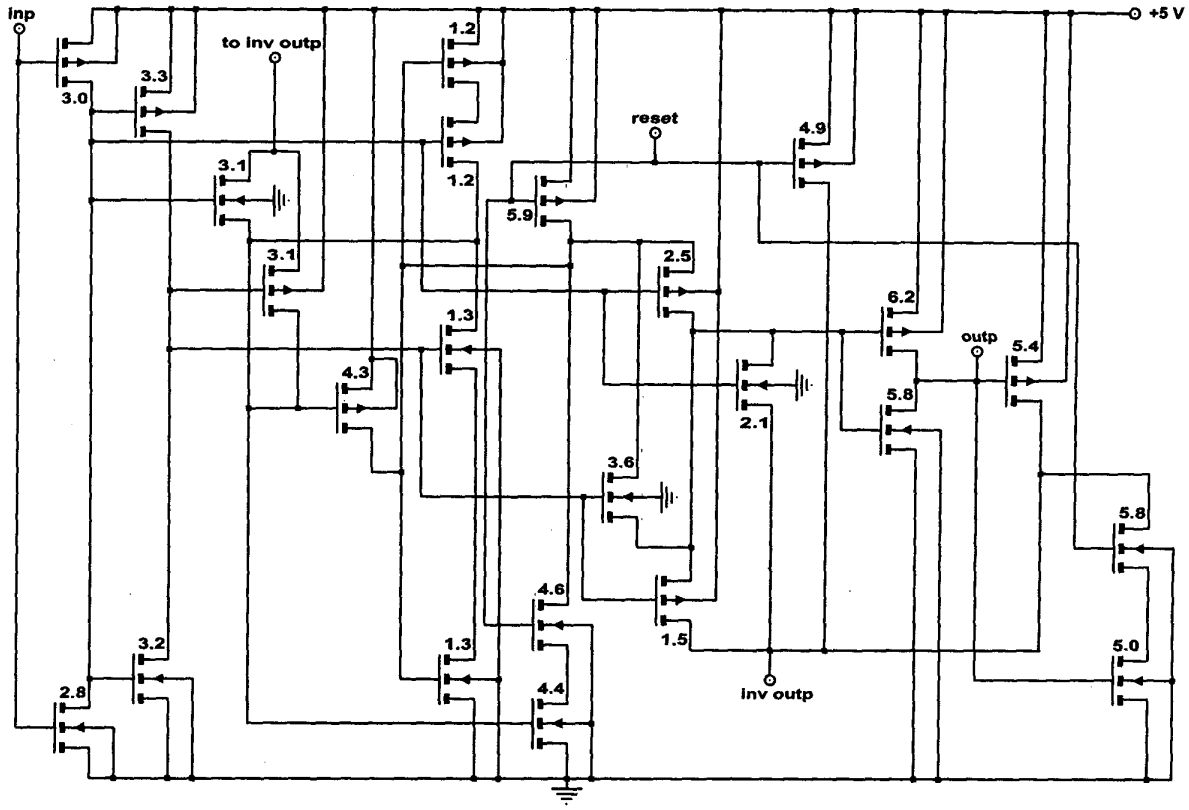

Fig. 3. The CMOS flip-flop circuit used as a sophisticated test of convergence—the numbers represent the SPICE "area" factors.

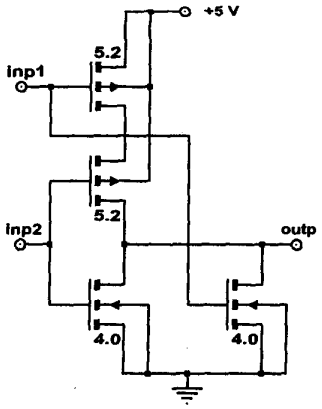

Fig. 4. The CMOS negative-or circuit that processes output of the two flip-flop circuits.

from the whole integrated circuit is necessary for testing. That circuit has caused serious convergence problems in SPICE analyses because it contains the transistors which alternate the sign of drain-source voltage during transient simulation. Hence, the analyses were tried by C.I.A. kernel.

A. About the Probed CMOS Subcircuits

The subcircuits are drawn in Fig. 3 and Fig. 4. Each of the transistors is labeled by SPICE area factor. Threshold voltages and other parameters of static model are determined for all the transistors from a technology parameter set.

Gate capacitors are defined by the equations (3) to (8) for the classical model and by updates (12) to (15) for the smoothed model—both are determined by (8) with oxide thickness 50 nm and several parameters of the static model modifying the voltage V_{on} and effective channel length.

The capacitance part of model is complemented by three (slight) gate overlap capacitors and—of course—by junction capacitors with zero-bias bottom capacitances 0.2 pF and zero-bias perimeter capacitances 0.05 pF.

B. About the C.I.A. Integration Algorithm

There is a derivation in [2] that some integration scheme (trapezoidal here) in conjunction with Meyer's model causes incorrect results for circuits with isolated nodes. Therefore, an algorithm choice for solving the circuit system

$$f(x(t), \dot{x}(t), t) = 0 \qquad (16)$$

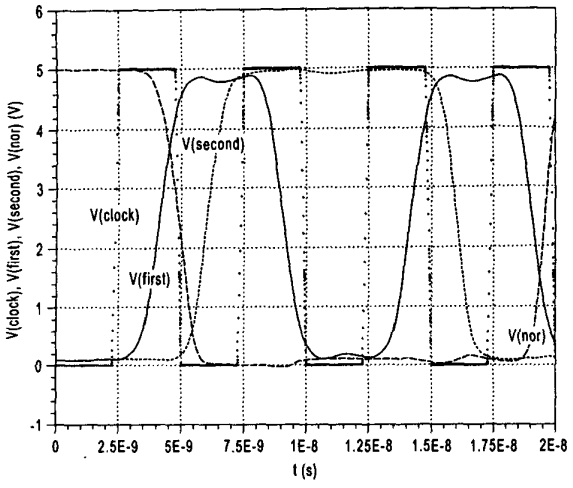

Fig. 5. Results of the test circuit—the first flip-flop circuit is switched by clock signal, the second is switched by the first one.

is also important for successful implementation of a model. A brief review of the C.I.A. algorithm is also necessary to explain advantages of the new model assessing its claims.

The C.I.A. algorithm uses backward scaled differences as an extrapolation (predictor) or interpolation (corrector) tool—they are defined for an n step by recursive formulae

$$\begin{aligned} \delta^{(0)}\boldsymbol{x}_n &= \boldsymbol{x}_n, \\ \delta^{(i)}\boldsymbol{x}_n &= \delta^{(i-1)}\boldsymbol{x}_n - \alpha_n^{(i-1)}\delta^{(i-1)}\boldsymbol{x}_{n-1},\ i=1,\ldots,k_n+2, \end{aligned} \tag{17}$$

where $\boldsymbol{x}_n = \boldsymbol{x}(t_n)$, k_n is an order of polynomial interpolation in the running integration step and

$$\begin{aligned} \alpha_n^{(0)} &= 1, \\ \alpha_n^{(i)} &= \alpha_n^{(i-1)}\,\frac{t_n - t_{n-i}}{t_{n-1} - t_{n-1-i}},\ i=1,\ldots,k_n+1. \end{aligned} \tag{18}$$

A prediction of values for a next chosen time t_{n+1} $\boldsymbol{x}_{n+1}^{(0)}$ is determined by the extrapolation using the differences (17)

$$\boldsymbol{x}_{n+1}^{(0)} = \sum_{i=0}^{k_n} \alpha_{n+1}^{(i)}\delta^{(i)}\boldsymbol{x}_n, \tag{19}$$

which is a more convenient form of Newton interpolation polynomial used here in an *explicit* form.

A correction of the values for t_{n+1} is determined using modified Newton iterations (limited in each of the integration steps by the algorithm's parameter "maxit")

$$\left[\left(\frac{\partial \boldsymbol{f}}{\partial \boldsymbol{x}}\right)_{n+1}^{(j)} + \gamma_{n+1}\left(\frac{\partial \boldsymbol{f}}{\partial \dot{\boldsymbol{x}}}\right)_{n+1}^{(j)}\right]\Delta\boldsymbol{x}_{n+1}^{(j)} = -\boldsymbol{f}_{n+1}^{(j)},\ j=0,\ldots \tag{20}$$

with the factor γ_{n+1} is to be derived from an *implicit* form of approximation of derivatives, which gives the formula

TABLE I

CONTRAST OF CLASSICAL AND SMOOTHED MODEL CLAIMS

type of gate capacity model	total number of non-convergen.	solutions of linear eqns.	LU-separations	logarithmic dampings
classical	5 (!)	3575	2903	987
smoothed	0	2484	1853	0

$$\gamma_{n+1} = \sum_{i=1}^{k_n} \frac{1}{t_{n+1} - t_{n+1-i}}. \tag{21}$$

After solving the system (20), $\boldsymbol{x}_{n+1}^{(\ldots)}$ and $\dot{\boldsymbol{x}}_{n+1}^{(\ldots)}$ are updated

$$\begin{aligned} \boldsymbol{x}_{n+1}^{(j+1)} &= \boldsymbol{x}_{n+1}^{(j)} + \Delta\boldsymbol{x}_{n+1}^{(j)}, \\ \dot{\boldsymbol{x}}_{n+1}^{(j+1)} &= \dot{\boldsymbol{x}}_{n+1}^{(j)} + \gamma_{n+1}\Delta\boldsymbol{x}_{n+1}^{(j)} \end{aligned} \tag{22}$$

but if an indication of divergence during the iterations (20) is detected then the logarithmic damping can be used

$${}^m\Delta x_{n+1}^{(j)} := \operatorname{sign}\left({}^m\Delta x_{n+1}^{(j)}\right)\left|{}^m x_{n+1}^{(j)}\right| \ln\left(1 + \frac{\left|{}^m\Delta x_{n+1}^{(j)}\right|}{\left|{}^m x_{n+1}^{(j)}\right|}\right) \tag{23}$$

for all the m components of $\Delta\boldsymbol{x}_{n+1}^{(j)}$ before using the (22).

C. About the Results With Classical and Smoothed Models

The TABLE I summarizes main differences between the analyses of the test circuit by the algorithm of subsection B. As expected and got by SPICE analyses too, the result by using classical models shows several nonconvergences —here, for 200 MHz clock signal with 250 ps rise and fall times, 5 nonconvergences occurred even for maxit = 200.

Moreover, the convergence problems cause a number of logarithmic dampings (23) to be used for classical model and (which is the worst) a quantity of LU factorizations of the Jacobian in (20) to be executed is considerably higher.

VI. CONCLUSION

The exponential smoothing for discontinuity elimination usable for both Meyer's and Ward's gate capacity model is suggested and tested on a sophisticated CMOS RFIC.

ACKNOWLEDGMENTS

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